

A SYNCHRONOUS FREQUENCY DIVIDER WITH ASTABLE MULTIVIBRATOR AS CLOCK CIRCUIT.

AMISHA SHYAM SAKHARE

Birla Vishvakarma Mahavidyalaya Engineering College, Vallabh Vidyanagar

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ABSTRACT:

This paper contains implementation of a Synchronous frequency divider with Astable multivibrator as clock circuit. The clock frequency of a digital system may not be suitable for operation. Hence, we may need to change it. Module performing this is called frequency divider. Counters can be used for this purpose. The clock pulses for this counter are produced by an Astable multivibrator. Astable multivibrator generally has a 50% duty cycle that produces a train of square wave pulses at a fixed known frequency.

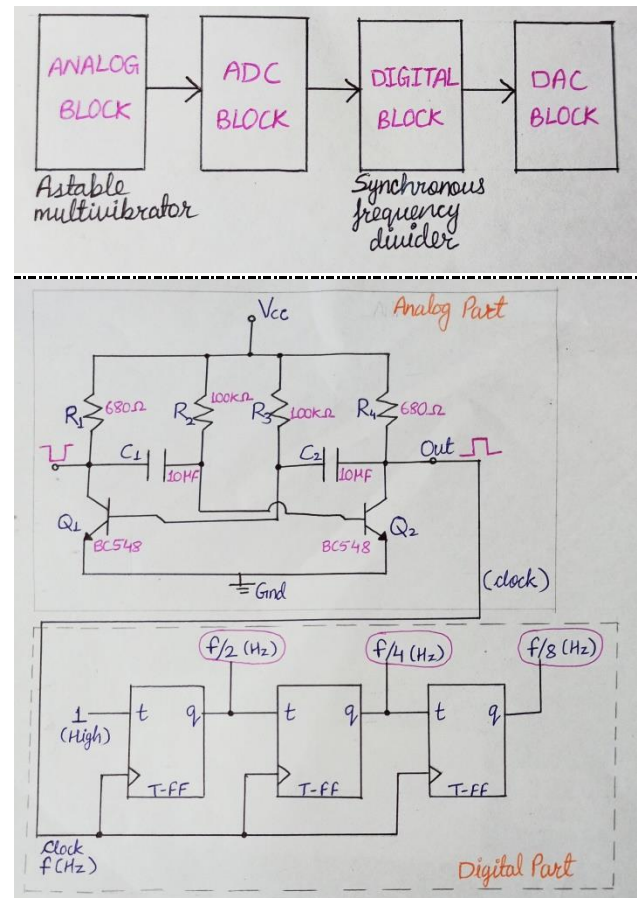
REFERENCE CIRCUIT DETAILS:

The T flip flops are useful when we need to reduce the frequency of the clock signal. If we use the original clock as flip flop clock and keep the T input at logic high then the output changes state once per clock period. This is with the assumption that the flip flop is not sensitive to both clock edges. This makes the output clock frequency as half of the frequency of the input clock. So the T flip flop works as a “Frequency Divider Circuit”.

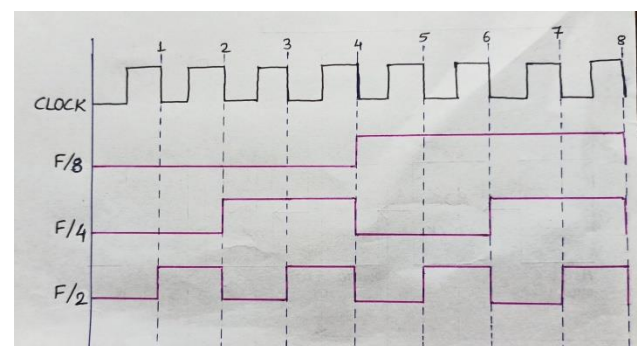
If we connect three T-type flip-flops, the initial input frequency will be “divided-by-two” by the first flip-flop ($f \div 2$) and then “divided-by-two” again by the second flip-flop ($(f \div 2) \div 2$), and then “divided by two” again by the third flip-flop ($((f \div 2) \div 2) \div 2$) giving an output frequency which has effectively been divided eight times, then its output frequency becomes one quarter value (12.5%) of the original clock frequency, ($f \div 8$).

The astable multivibrator circuit consists of two switching transistor, a cross-coupled feedback network and two time delay capacitors which allows oscillation between the two states with no external triggering to produce the change in state. The time period is determined by the time constant of the RC networks connected across the base terminals of the transistor. As the transistors are switching both “ON” and “OFF”, the output from either collector will be a square wave with slightly rounded corners because of the current which charges the capacitors. If the value of the capacitor $C_1=C_2$ and also the value of base resistor $R_2=R_3$ then the total length of time of the Multivibrator cycle is symmetric (duty cycle = 50%).

REFERENCE CIRCUIT DESIGN:



REFERENCE WAVEFORMS:



REFERENCES:

- (1) <https://dcaclab.com/blog/t-flip-flop-explained-in-detail/>
- (2) <https://www.electronics-tutorials.ws/waveforms/astable.html>